查询IRF1010EL供应商

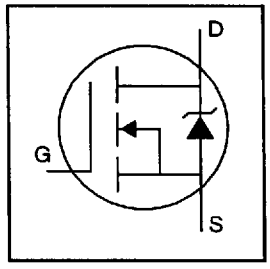
International
IOR Rectifier

PD - 9.1720

IRF1010ES/L

HEXFET® Power MOSFET

- Advanced Process Technology
- Surface Mount (IRF1010ES)
- Low-profile through-hole (IRF1010EL)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



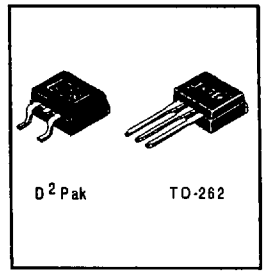
V_{DSS} = 60V

$R_{DS(on)}$ = 0.012Ω

I_D = 83A⑥

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications. The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRF1010EL) is available for low-profile applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑤	83⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑤	59	
I_{DM}	Pulsed Drain Current ①⑤	330	
P_D @T_A = 25°C	Power Dissipation	3.8	W
P_D @T_C = 25°C	Power Dissipation	170	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	320	mJ
I_{AR}	Avalanche Current①	50	A
E_{AR}	Repetitive Avalanche Energy①	17	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.90	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)**	—	40	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.06	—	V/°C	Reference to 25°C, I_D = 1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.012	Ω	V_{GS} = 10V, I_D = 50A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	36	—	—	S	V_{DS} = 25V, I_D = 50A⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 60V, V_{GS} = 0V
		—	—	250		V_{DS} = 48V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	116	nC	I_D = 50A
Q_{gs}	Gate-to-Source Charge	—	—	23		V_{DS} = 48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	47		V_{GS} = 10V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 30V
t_r	Rise Time	—	90	—		I_D = 50A
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		R_G = 3.6Ω
t_f	Fall Time	—	71	—		R_D = 0.60Ω, See Fig. 10 ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	2800	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	880	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	290	—		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	83⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	330		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 50A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	70	110	ns	T_J = 25°C, I_F = 50A
Q_{rr}	Reverse Recovery Charge	—	200	300	nC	di/dt = 100A/µs ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 260µH R_G = 25Ω, I_{AS} = 50A. (See Figure 12)

③ I_{SD} ≤ 50A, di/dt ≤ 260A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle £ 2%.

⑤ Uses IRF1010E data and test conditions

⑥ Caculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

** When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended soldering techniques refer to application note #AN-994.

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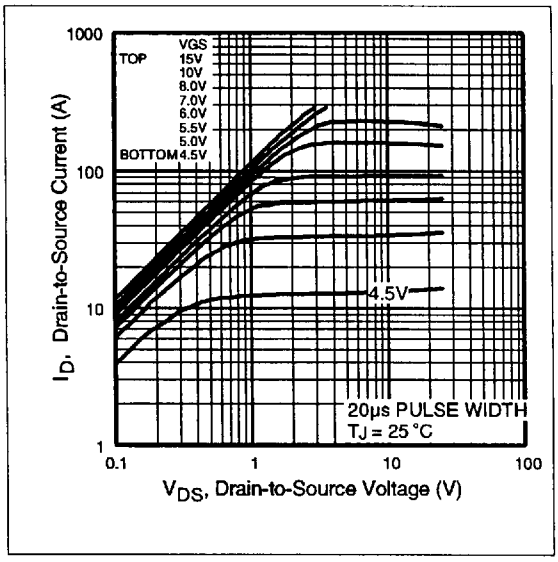

Fig 1. Typical Output Characteristics

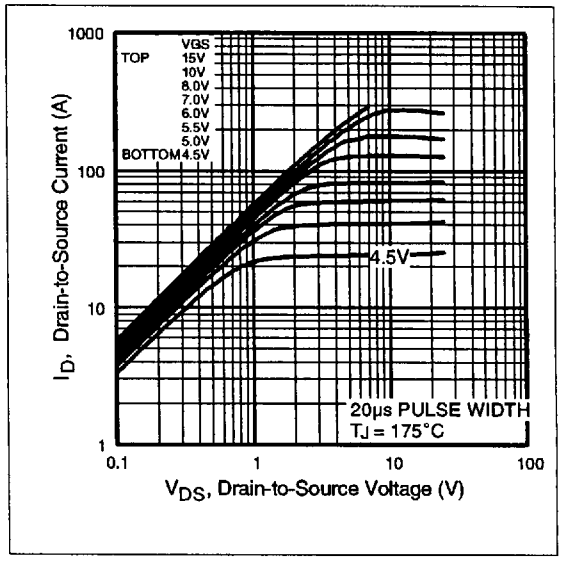

Fig 2. Typical Output Characteristics

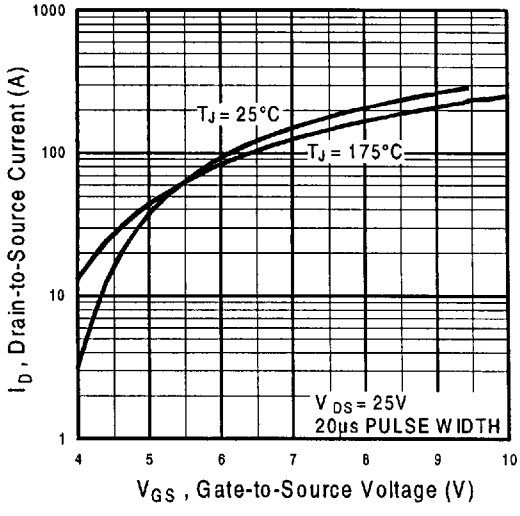

Fig 3. Typical Transfer Characteristics

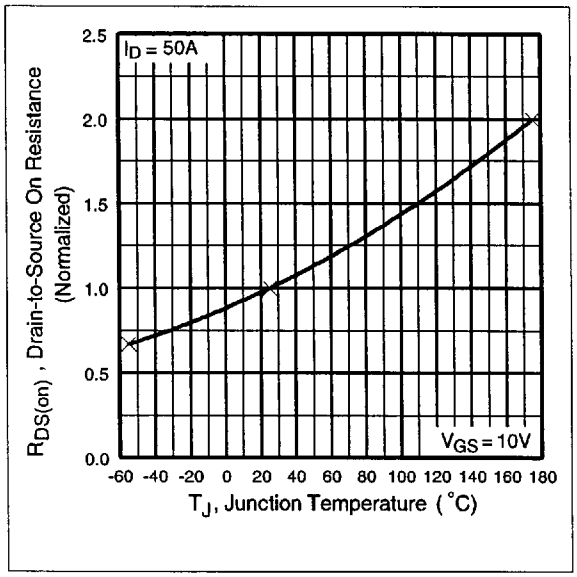

Fig 4. Normalized On-Resistance Vs. Temperature

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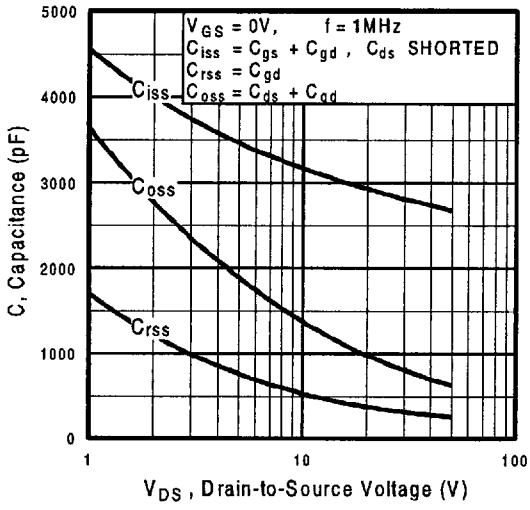

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

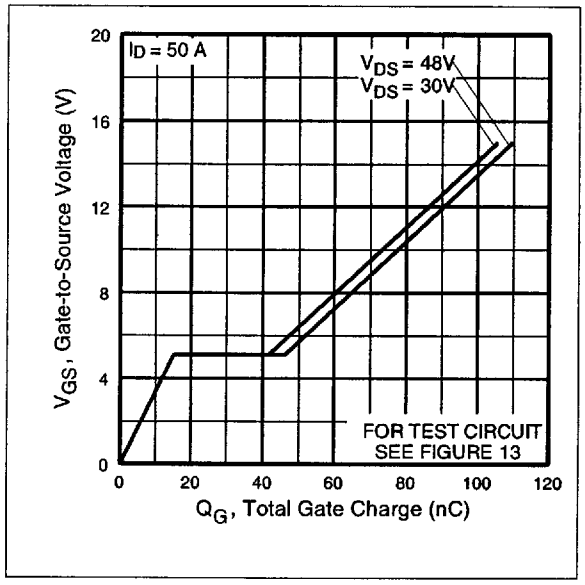

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

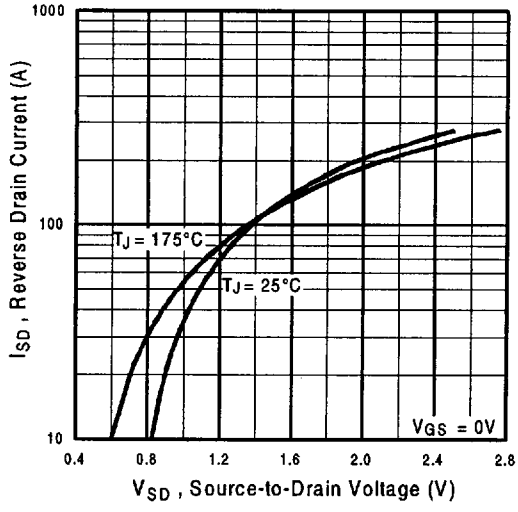

Fig 7. Typical Source-Drain Diode Forward Voltage

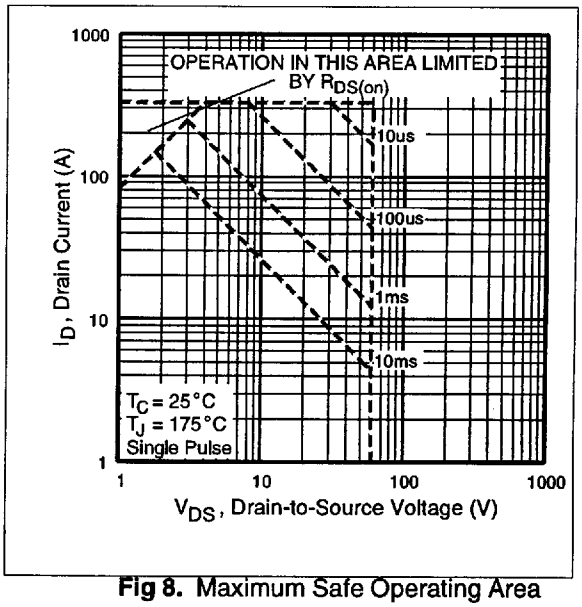

Fig 8. Maximum Safe Operating Area

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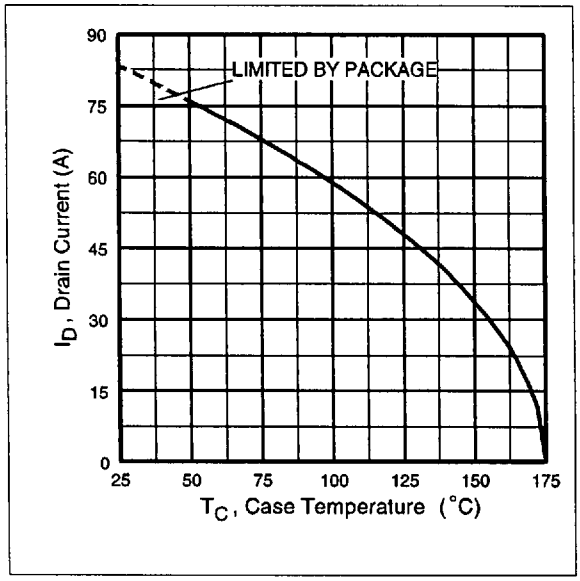

Fig 9. Maximum Drain Current Vs. Case Temperature

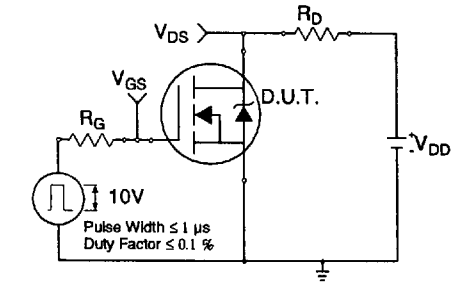

Fig 10a. Switching Time Test Circuit

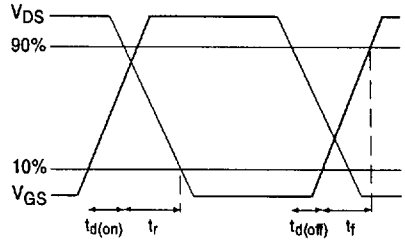

Fig 10b. Switching Time Waveforms

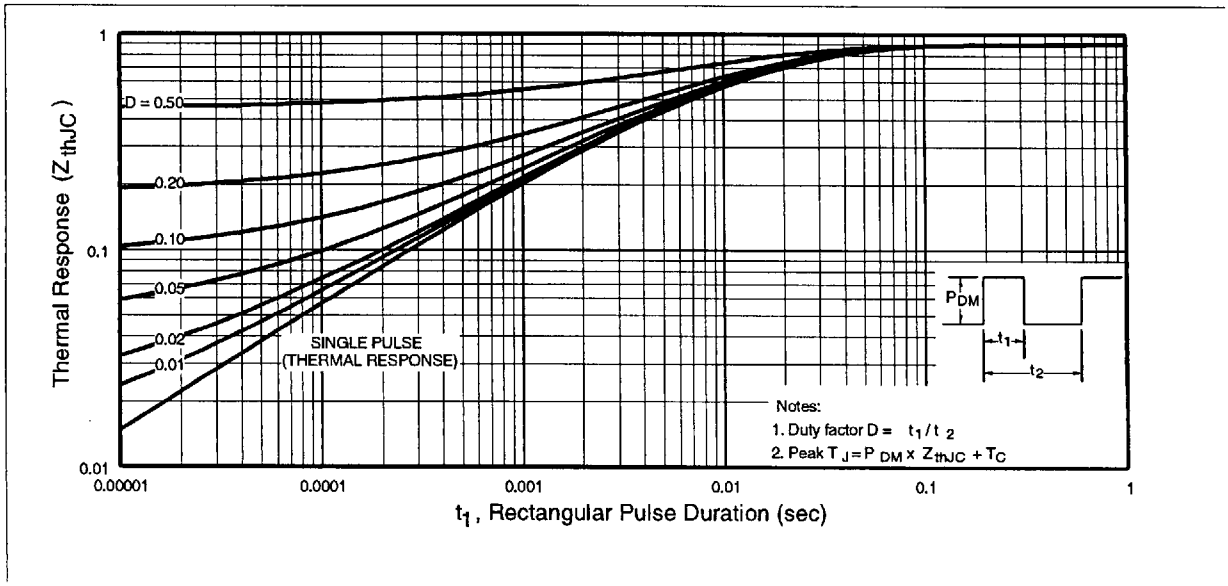

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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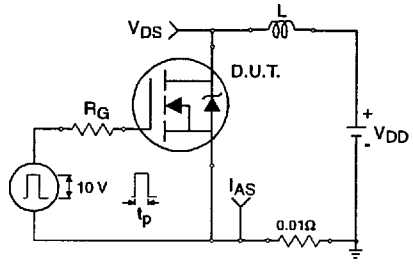

Fig 12a. Unclamped Inductive Test Circuit

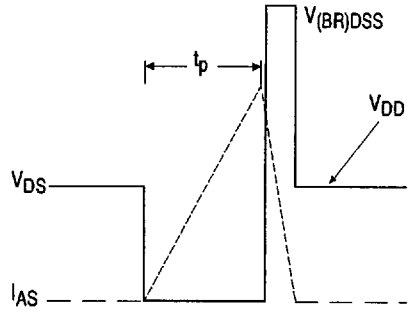

Fig 12b. Unclamped Inductive Waveforms

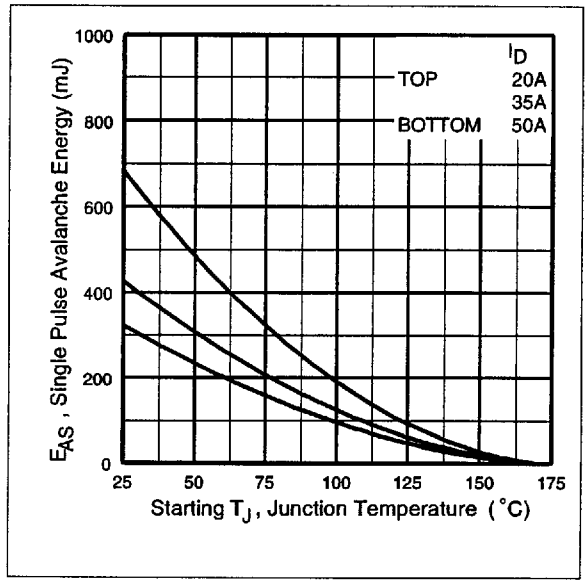

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

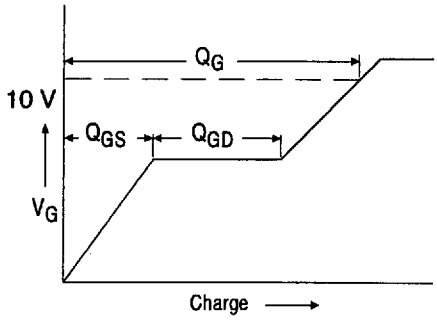

Fig 13a. Basic Gate Charge Waveform

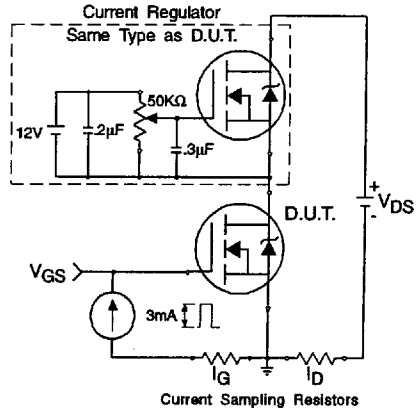

Fig 13b. Gate Charge Test Circuit

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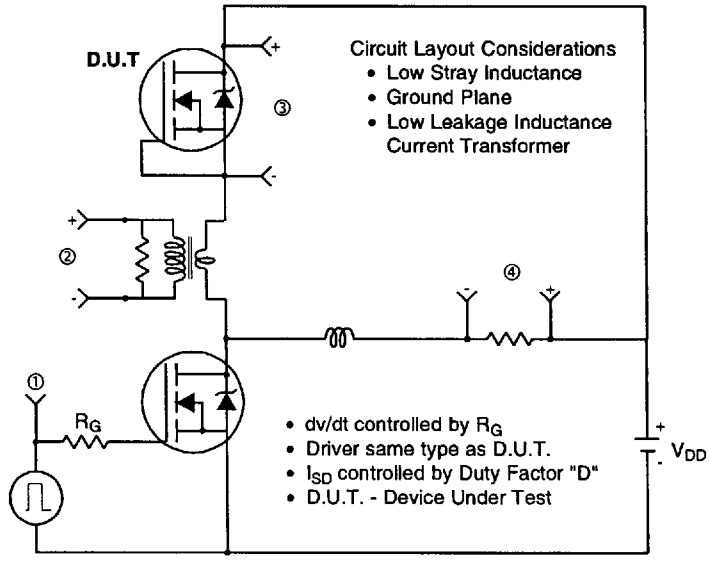
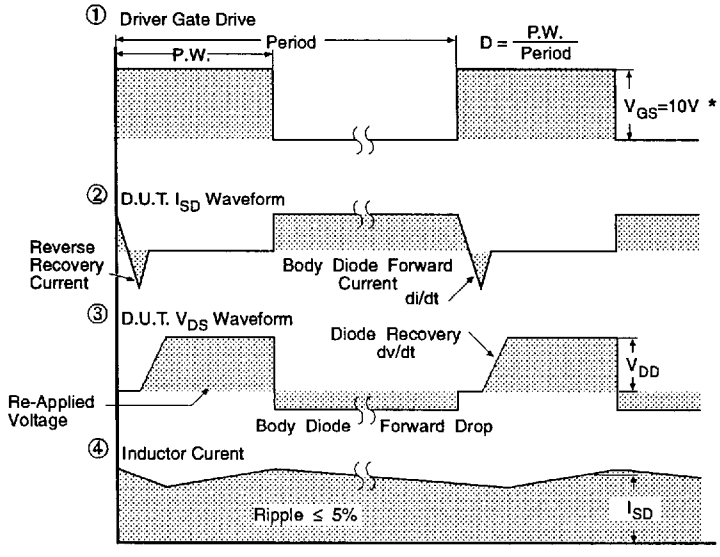
Peak Diode Recovery dv/dt Test Circuit





* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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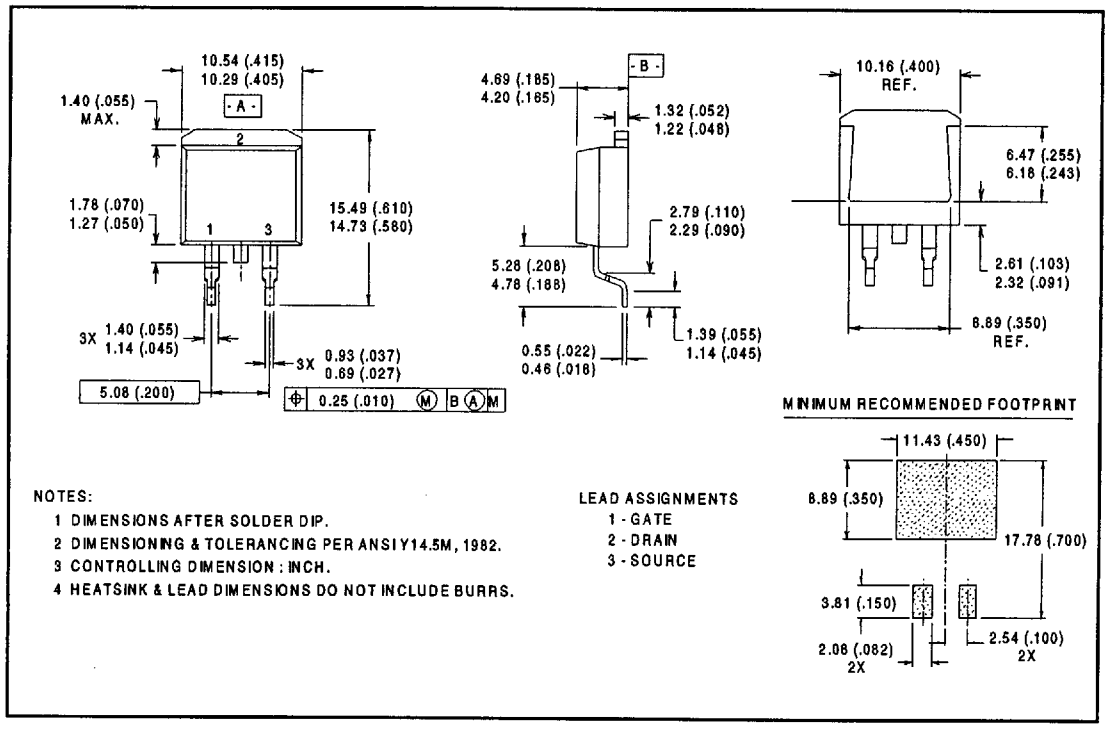
D²Pak Package Outline

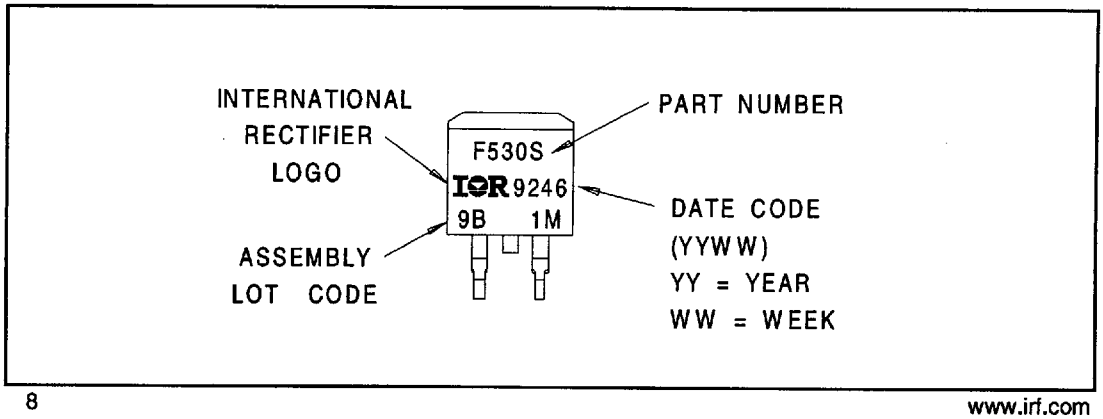


NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

Part Marking Information

D²Pak



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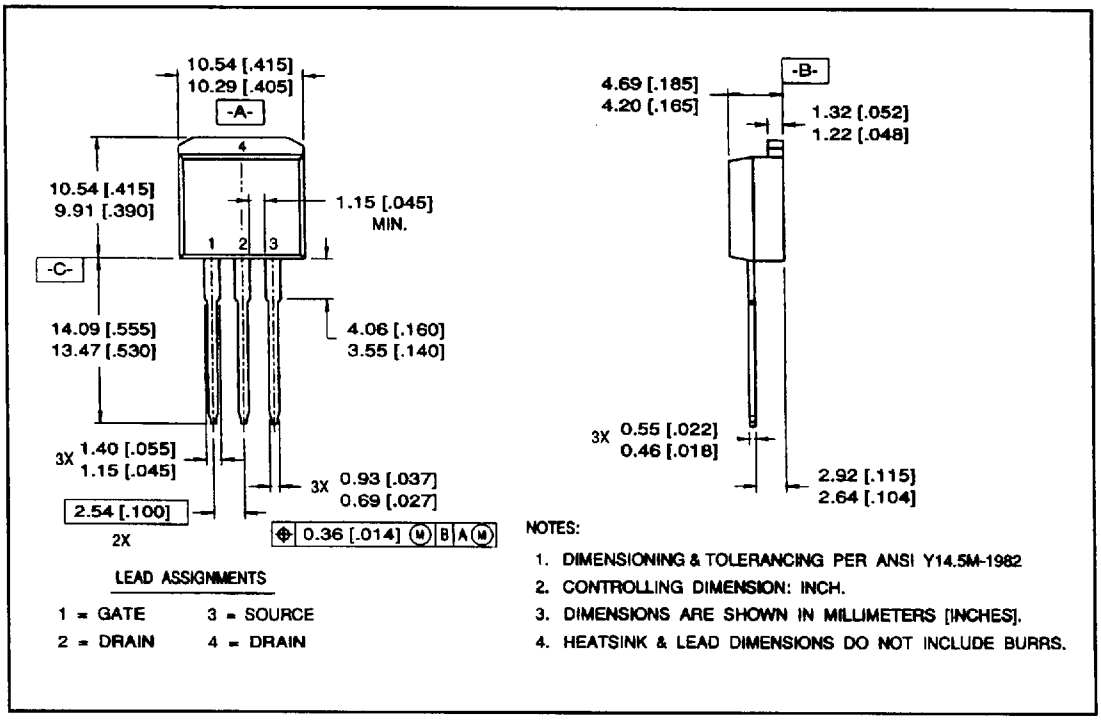
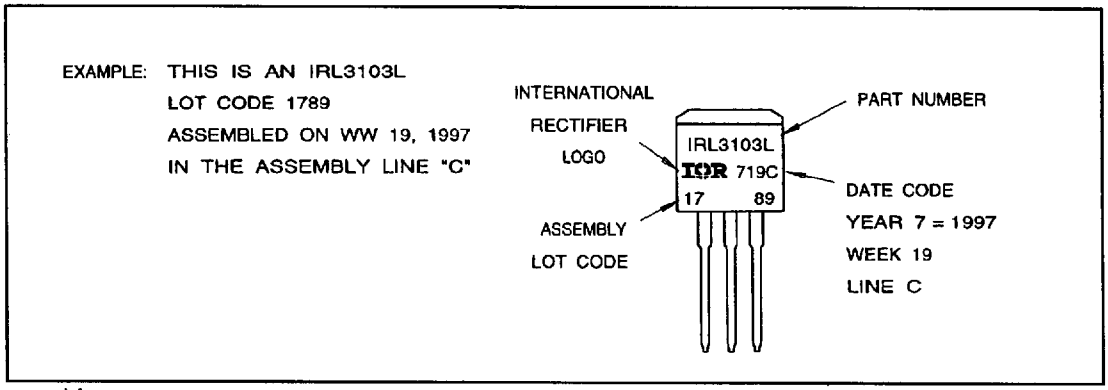
Package Outline

TO-262 Outline



Part Marking Information

TO-262



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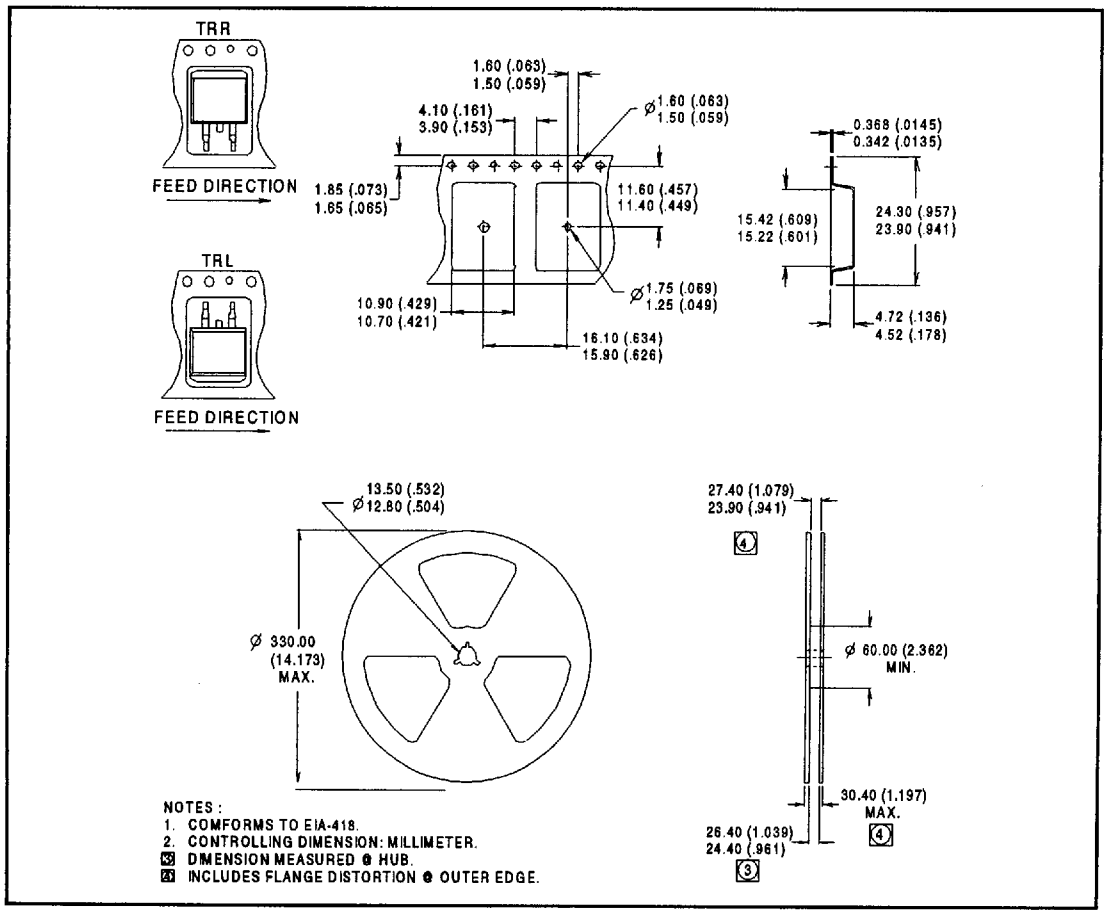
Tape & Reel Information

D²Pak



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
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